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INVENTIVE DISCLOSURE - CONFIDENTIAL

1. **Proposed Title of the Invention**:
   A Novel Pulse-Transformer for Isolated Gate Driving of Parallel Connected SiC Mosfets in Induction Cap Sealing Applications.

2. **Proposed Abstract of the Invention**

Induction heating principle is used for sealing of bottles filled with diverse products, e.g., pharmaceutical, petroleum, nutraceuticals, food and beverage items, etc. Using the energy transferred contactless to thin AL foil the induction sealing ensures the bonding of foil with container's lip. The process could use continuous-run controller or switched ON when desired. Single-switch power controller is used for ON-OFF mode controller, where parallel resonant tank circuit is energized every switching cycle by large-current short pulse to enable transfer of requisite energy to the foil. To increase the productivity in ON-OFF mode, as required by capless sealing process, both ON and OFF time of the controller are kept small. It requires higher capacity controller with better thermal management. To reduce the power loss with improved thermal faetures, this invention proposes to use two SiC Mosfets for the switch. Unlike Si based devices, gates of SiC Mosfets mandatorily require bi-polar gate voltage. They need high gate voltage for turn-on, and mandatorily certain negative bias for turn-off. They are sensitive to transient gate voltages. They not only need narrow-band asymmetrical gate voltage (e.g., +20V/-5V), the band could be different for suitable alternates. For the first time, this invention proposes to use a novel pulse-transformer based gate drive circuit for driving isolated gates of parallelly connected SiC Mosfets for single-switch power controller for induction cap sealer.

3. **Key Words:**
   Induction cap sealing controller; pulse-transformer based gate drive circuit, transformer leakage inductance, transformer winding configuration; SiC Mosfet.

4. **Background of the Invention:**

What are the present technologies that exist in the field of your invention and what are the limitations of the same?

Sealing of plastic or glass containers could be the most popular application domain of IH principle [1-5]. Here, transferred energy to a thin AL foil is used for sealing containers having different foil dimension (Fig. 1). For high-speed sealing, the process is set on-line where the power converter is continuously kept on. For sealing smaller quantity, ON-OFF type single switch controller [6] is used (Fig. 2). The speed of production could be increased if the power rating of the controller is increased, and/or through better thermal design. Often, capless induction sealer uses high-speed sealer in ON-OFF mode. In modern packaging, the role of capless induction sealer is important. In traditional induction cap sealing process, using paraffin wax, a cardboard placed inside the cap is used to hold a thin foil. The mandatory wax removal process slows down the speed of sealing to a certain extent. It is difficult to perform quality check of each sealed containers whose top is covered by a cap. The process could generate following quality issues:

1. Overheating/burning on certain area of the foil
2. Under sealing or less heating
3. Incomplete wax removal, etc.

Fig. 1: Sealed containers using induction heating principle.

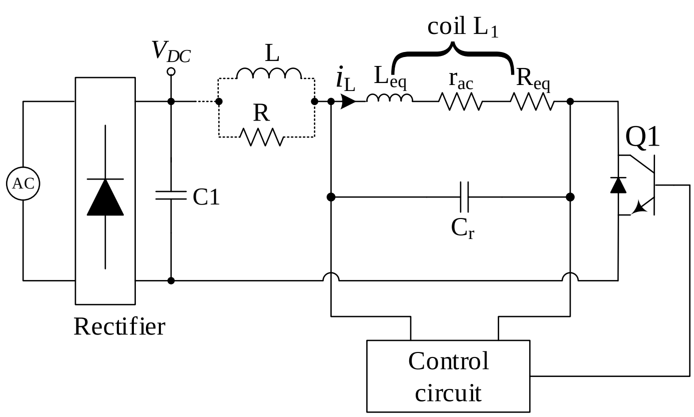


Fig. 2: Basic diagram of single-switch converter for induction cap sealing

The mechanism of checking the quality of sealing of each container indirectly is not only cumbersome, it would be error-prone, extremely costly and sluggish. In order to have better and direct quality check of each sealed container in a simple, and cost-effective way, the emerging trend is to migrate to capless induction sealing where the role of power converter is critical. Ideally, it should be compact and light weight where single switch topology could be ideal. One typical single-switch induction heating controller is shown in Fig. 2.

Minimally, its tank-circuit consists of inductor L1 and capacitor C_r. In this automated process the coil L1 is energized only when the coil head holding a bare foil is perfectly engaged to the lip of the container. For high-speed sealing both the ON and OFF time of the controller is kept small, almost like a continuous duty use. The converter does not have any power control circuit. The quantum of energy transferred to the foil is controlled by changing the duration of ON time of each sealing cycle. The bulk of power loss in the converter takes place in L1 and Q1 [5]. For L1, it is spatially distributed. Whenever energized, the presence of foil underneath significantly reduces the impact of proximity effect on its power loss. The reduction of power loss in Q1 is a concern.

The power P_{OUT} transferred electro-magnetically to a foil is expressed as,

$$P_{\mathrm{OUT}} = i_L^2 R_{eq} \tag{1}$$

L1 is the inductance of coil head and i_{L} is the coil current of frequency f_{s}. R_{eq} represents the load resistance R_{foil} of a foil reflected to the tank circuit, it is expressed as [5],

$$R_{\mathrm{eq}} = \frac{\omega_s^2 M^2 R_{\mathrm{foil}}}{R_{\mathrm{foil}}^2 + \omega_s^2 L_{\mathrm{foil}}^2} \tag{2}$$

L_{foil} is foil inductance and R_{foil} is the resistance of the foil, M is the mutual inductance between the coil and foil and $\omega_s = 2\pi f_s$. For a particular value of R_{foil}, the value of R_{eq} could be increased by increasing the frequency f_{s}. When the coil holding the foil is energized, the current drawn by the foil would reduce the value of inductance from L1 to, say, L_{eq}, like,

$$L_{\mathrm{eq}} = L_1 - \frac{\omega_s^2 M^2 L_{\mathrm{foil}}}{R_{\mathrm{foil}}^2 + \omega_s^2 L_{\mathrm{foil}}^2} \tag{3}$$

The loading of coil not only reduces the value of L1, the effective resonant frequency f_{s} of the tank circuit is increased, because,

$$f_{\mathrm{s}} = \frac{1}{2\pi\sqrt{L_{\mathrm{eq}} C_r}} \tag{4}$$

4.1 Single-Switch Induction Sealer

The frequency of ON-OFF operation of induction sealer is desired to be high; it needs to be equipped like a continuous run converter. The loading pattern of the power converter is complex. The value of R_{eq} varies widely; its value is zero at no load when there is no foil beneath the coil. The value of R_{eq} changes with the diameter of the foil. Depending upon the load conditions, the value of time constant τ of current envelope drifts between its maximum and minimum values [5], like,

$$\tau_{\mathrm{max}} = \frac{2L_1}{r_{\mathrm{ac}}} \quad \text{and,} \quad \tau_{\mathrm{min}} = \frac{2L_{\mathrm{eq}}}{r_{\mathrm{ac}} + R_{\mathrm{eq}}} \tag{5}$$

Here, r_{ac} is the ac resistance of the coil L1. When compared with the loading of other applications (e.g., induction cooking), due to very thin (10-20 μm) AL foil considered as load, the value of the R_{eq} is not large; the condition $\tau_{\mathrm{min}} \gg 1/f_{\mathrm{s}}$ is true. For such load range, the current i_{L} would be sinusoidal (Fig. 3) and remains continuous even by momentary charging of capacitor Cr in each cycle. The expression of voltage across Q1 is,

$$V_{\mathrm{CE}} = V_{\mathrm{DC}} - V_{\mathrm{Cr}} \tag{6}$$

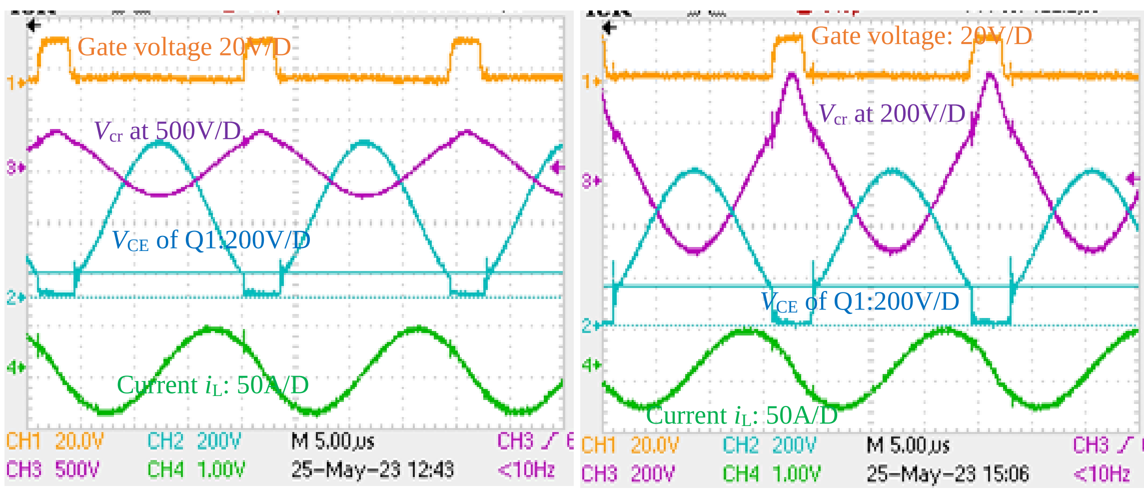
The charging of tank-circuit should not incur large power loss in Q1. To eliminate the turn-on loss, if Q1 is turned on at zero voltage then the power is transferred to the tank circuit mostly via L1. The peak value of current light-load applications could be large, predominantly decided by r_{ac} and the current limiter (Fig. 2). The associated large power loss in Q1 could either effect thermal shut-down of the converter or damage the switch. Moreover, if the value of V_{CE} is large at turn off, then apart from significant power loss during turn-off. For uncertain wide range value of $r_{\mathrm{ac}} + R_{\mathrm{eq}}$ as load, the requisite energy E_{tank} is transferred to the tank circuit predominantly through charging of Cr in each cycle of frequency f_s. It is possible when the voltage V_{CE} is positive, i.e., near zero voltage switching condition. E_{tank} could be expressed as,

$$E_{\mathrm{tank}} = \frac{1}{2} C_{\mathrm{r}} (V_{\mathrm{DC}}^2 - V_{\mathrm{Cr-on}}^2) \tag{7}$$

$(V_{\mathrm{DC}} - V_{\mathrm{Cr-on}})$ is the voltage across Q1 at turn-on instant. When Q1 is turned off, the tank-circuit is decoupled from the supply. The waveforms of the converter (Fig. 2) at two different preset values of V_{CE} for turn-on are shown in Fig. 3. It used three high-speed low-loss IGBTs (Table 1). The value of f_s of unloaded tank circuit was 53 kHz. The profile of current I_{Q1} in Q1 for charging the Cr could be derived from (8), like,

$$\int_0^{DT_{\mathrm{p}}} I_{\mathrm{Q1}} dt = (V_{\mathrm{DC}} - V_{\mathrm{Cr}}) C_{\mathrm{r}} \tag{8}$$

D is the duty cycle in a full cycle period $T_P = 1/f_s$.



a) b)

Fig. 3: Waveforms of an IGBT based single-switch power controller for induction sealing when Q1 is turned on at, a) 96V and, b) 152V.

4.2 Selection of Switching Device

The selection of a device for Q1 is based on power loss in it, voltage stress, temperature rise in it, ease of gate driving and cost. The cost includes the price of the device, associated heat sink and gate drive, area of PCB consumed. In each switching cycle the peak value of V_{CE} (6) appears when Q1 is in turned-off condition (Fig. 3). The voltage rating of the device should be 1200V, they are commonly available. The turn-on time of Q1 in each cycle is small, ideally, just sufficient to charge C_r to V_{DC}. The peak device current for charging Cr is large. Though there could be a certain voltage across Q1 during turn off, the current through it would ideally be small.

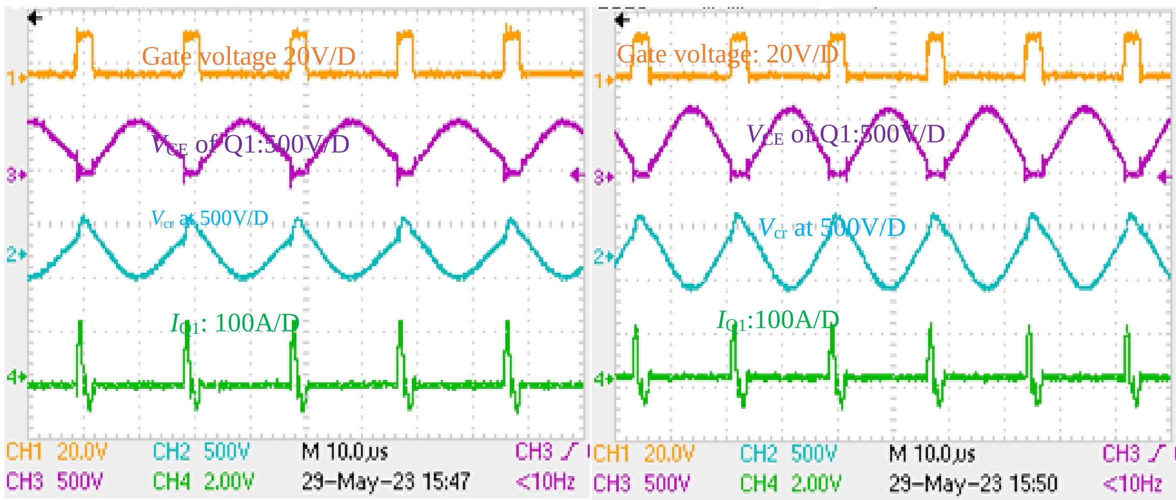
The power loss P_L in Q1 consists of conduction loss P_{cond} and switching loss P_{sw}, like,

$$P_L = P_{\mathrm{cond}} + P_{\mathrm{sw}} = P_{\mathrm{cond}} + f_s E_{\mathrm{sw}} \tag{9}$$

P_{cond} depends on conduction drop, current profile and duration D/f_s. The switching energy loss E_{sw} consists of turn-on loss E_{on}, turn-off loss E_{off} in Q1 and reverse recovery loss E_{rr} in anti-parallel diode. The value of each loss component depends on the value of current and voltage at the switching instant and the junction temperature T_j. For effective transfer of power of desired value (1), the value of f_s is kept large (2). It is decided by the tank circuit parameters L1 and Cr. The turn-on time DT_p of Q1 is kept small. The T_j of a device is expressed as,

$$T_j = T_{amb} + R_{th} P_L \tag{10}$$

T_{amb} is ambient temperature, R_{th} is the thermal resistance of the device and the heat sink.



a) b)

Fig. 4: Waveforms of IGBT based power controller while sealing, a) 55 mm dia. foil, and, b) 95 mm dia. foil. [for current limiter a 0.8 µH inductor was used].

Table 1: Features of the single switch converter: three IGBTs vs two SiC Mosfets.

	IGBT	SiC Mosfet
Device Q1	STGW40H120DF2	ACM020P120Q
Device rating at T_c=100 ^{0}C	40A, 1200V	71A, 1200V
Gate threshold voltage, V_{gth}, V	6.0	1.8
Switching frequency f_s, kHz	60	60
No. of devices in parallel	3	2
Peak current per device, A	36	54
Total power loss in Q1, W	112	52

Fig. 4 shows waveforms of the inverter including the current through Q1 for two different sealing applications. The value of peak current was 108 A. Three number of high-speed low-loss IGBTs (STGW40H120DF2) were used for Q1. They were driven by a single non-isolated unipolar gate drive circuit (GDC). The value of L1 was 18µH and that of Cr was 0.5µF. In each cycle, Q1 was turned on for 3µs. The calculated value of P_L of IGBT assembly for Q1 is listed in Table 1. It also shows that if IGBT assembly is replaced by two SiC Mosfets, there would be drastic reduction in power loss [7-10]. SiC Mosfet based converter would be more appropriate for near continuous-duty capless induction sealing applications. Though they appear to be superior for high-frequency large-current pulse charging applications, there could be increased complexity to design a GDC for generating noise-free desired asymmetrical gate voltages with narrow pulse width accurately to drive multiple SiC Mosfets in parallel [11-17]. It should have following features:

1. Proper galvanic isolation for effective use of Kelvin source terminals to decouple the power circuit from the sensitive low-voltage control circuit
2. Feed bi-polar asymmetrical gate voltage devoid of any ringing or oscillations
3. Negligible propagation delay, rise and fall time, and,

It should be simple, low cost with minimum component count.

5. Detailed Explanation of the Invention along with working examples. Kindly provide an elaborated description of each and every aspect of the invention in great detail.

It was clear from two experimental results of Fig. 4 that IGBTs were turned-off at zero current but at certain voltage across Q1. Though multiple (three) IGBTs were driven by a common unipolar GDC, gate signals were devoid of any noise or oscillations. On several fronts, the gate requirement of Si devices is different from that of SiC Mosfets [11]. It has been standardized for Si devices. They are turned-on at relatively small voltage (≤15V). Depending upon the power circuit configuration, they could be turned-off by applying wide-range of negative bias, it could be zero voltage as well (Fig. 4). The ratio of limiting value of gate voltage for turn-on (30V) and turn-off (-30V) is 1, there exists a large operating gap between the nominal operating and limiting values. Such flexibility makes Si devices naturally compatible to PT-based GDC for wide range duty cycle [18], [19]. Generally, just a change in gate resistor is needed to accommodate a suitable alternate.

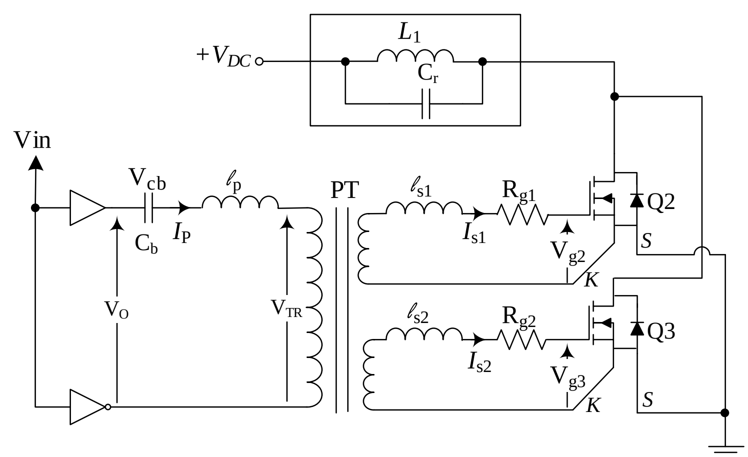


Fig. 5: Diagram of a PT based GDC for driving two SiC Mosfets in parallel.

On the other hand, gate voltage requirement of SiC Mosfets are device specific (e.g., refer to data sheets of ACM020P120Q, IMZA120R020M1H, etc.), influenced by several parameters such as gate threshold voltage, transconductance, device capacitances, dV_{ds}/dt, etc. They are turned-on at high gate voltage (≥18V) and turned-off by mandatorily applying certain negative bias (≤ -5V). The ratio of limiting value of gate voltage for turn-on (+25V) and turn-off (-10V) is large (>1). Compared to Si devices, the respective operating boundary is constrained. The GDC should be able to generate the desired asymmetrical gate voltage accurately. As it operates on flux balancing principle in the core, primary-driven completely passive PT-based GDC apparently appears to be less suitable. The complexity further increases when, to avail the kelvin source terminals, several parallel devices are driven in isolated manner. For proper current sharing by multiple devices, multi-winding PT must ensure equal dynamic gate voltage in each gate. Lastly, due to their small value of gate threshold voltage, the gate voltage should be devoid of any oscillations to avoid spurious turn-on of SiC Mosfets.

5.1 PT Based Gate Drive for Parallel Connected SiC Mosfets

The pulse-transformer based GDC is shown in detail in Fig. 5. A DC blocking capacitor C_b is added to avoid any magnetic saturation in PT. With two secondary windings, its turns-ratio is 1:1:1. Ideally, the primary voltage would be reflected at the secondary terminals. When the device is desired to be turned-on for duration DT_p, at supply voltage V_{cc}, the primary voltage V_{TR+} of PT could be expressed as [12],

$$V_{TR+} = 2V_{cc}(1 - D) \quad (11)$$

During turn-off interval $(1 - D)T_p$, primary voltage V_{TR-} is,

$$V_{TR-} = 2V_{cc}D \quad (12)$$

For majority of SiC Mosfets, permissible range of turn-on voltage is $18V \leq V_{TR+} \leq 25V$, and that of turn-off voltage is $-2V \geq V_{TR-} \geq -10V$. When the value of f_s changes with load (4) or application, value of D would also shift. Therefore, both V_{TR+} and V_{TR-} would drift with f_s. For induction sealing the converter operates in a frequency range $40k\text{Hz} \leq f_s \leq 80k\text{Hz}$. Considering the on-time DT_p is kept at constant at 3 µs, Table 2 shows the operating gate voltage V_{TR+} and V_{TR}. Though differently, the operating margin of V_{TR+} and V_{TR-} changes with f_s. When f_s is small, not only the operating margin for V_{TR+} is constrained, small value of V_{TR-} could make the gate susceptible to spurious turn-on. Therefore, GDC needs to be accurate for proper functioning of the converter over a large band of f_s.

Table 2: Asymmetrical gate voltage over the frequency band of induction sealing converter

Frequency f_s, kHz	40.0	50.0	60.0	70.0	80.0
V_{cc}, V	12.5	12.5	12.5	12.5	12.5
Total period T_p, µs	25.0	20.0	16.7	14.29	12.5
Duty cycle, %	12.0	15.0	18.0	21.0	24.0
V_{TR+}, V	22.0	21.25	20.5	19.75	19.0
V_{TR-}, V	-3.0	-3.75	-4.5	-5.25	-6.0

To generate the desired asymmetrical gate voltage accurately over wide frequency range, the multi-secondary PT needs its each winding to possess large self-inductance, say, L_s and small value of leakage inductance l_{lk}. The coupling coefficient $k = \sqrt{1 - l_{lk}/L_s}$ of each winding should be large.

5.2 Preliminary Results Using Commercial PTs Suitable for Si IGBTs and Mosfets

The single-switch power converter (parameters are listed in Table 3) was designed tested using two commercially available high-frequency PTs from reputed manufacturers. Both are popular for driving Si IGBT or Mosfet. The frequency range of induction sealer falls within the operating frequency band of both the PTs, their parametric details are listed in Table 3. Apparently, the value of k between any two windings of PT1 and that in PT2 was large (> 0.999).

Table 3: Parameters of the converter for conducting experiments

Inductance L1, µH	18.0
Tank capacitor Cr, µF	0.5
Device Q2, Q3	ACM020P120Q
Gate resistor R_{g1}, R_{g2}, Ω	5.0
Turn-on duration DT_p, µs	3.0
Operating range of f_s, kHz	40-80

Table 4: Parameters of two commercial pulse transformers

	PT I	PT 2
Model	SIRIO T117323	VAC 4097X058
V.µs rating	140	260
Turns ratio	1:1:1	1:1:1
Isolation voltage, *k*V	4.0	3.1
L_p, L_{s1} and L_{s2}, mH	0.314, 0.311, 0.303	5.8, 5.79, 5.79
l_{pl}, l_{s1}, l_{s2}, nH	335, 360, 380	400, 410, 418
Coupling coeff., *k*	0.9993	0.9999
Inter winding cap., pF	≈38	≈40

Note: L_p, L_{sl}, L_{s2}: Self-inductance of primary and two secondary windings and l_{pl}, l_{s1}, l_{s2} are respective values of l_{lk}.

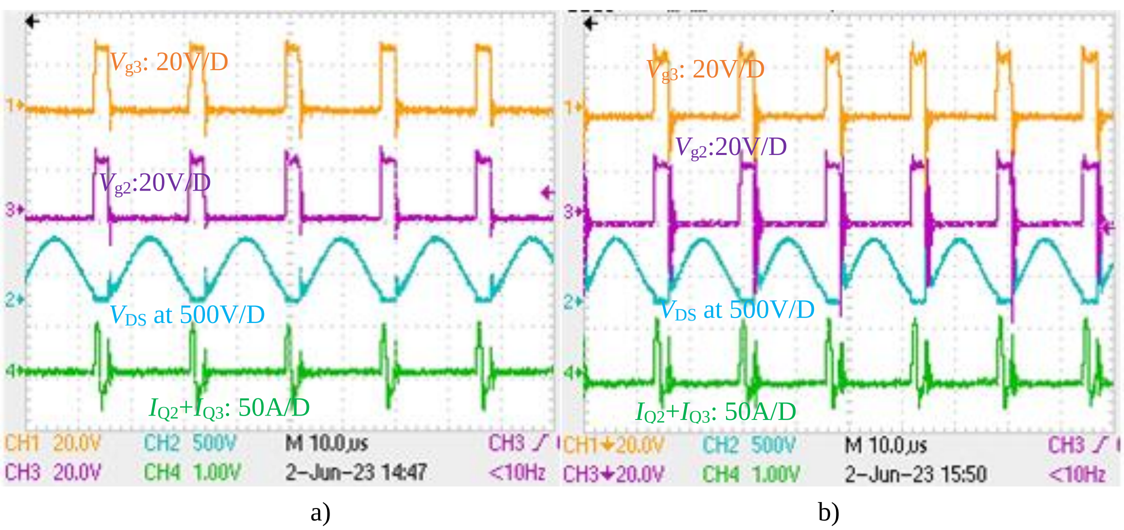


Fig. 6: Even when the coil was not loaded, large ringing in gate voltages during turn-off effected spurious turn-on of SiC Mosfets while using, a) PT1, and, b) PT2.

To understand the role of different parameters of magnetically powered GDC to drive two SiC Mosfets in parallel, a power converter was designed to accommodate both the PTs. Fig. 6a shows the waveforms of gate voltages while using PT1, and also the current and voltage in Q1 while driving a tank circuit for induction sealing. It is clear that during the turn-off of Q1, there was spurious turn-on that resulted current flow through the devices. Though, the values of both L_s and *k* were more for PT2, its performance was worse even at lighter load condition (Fig. 6b); the value of l_{lk} was more for PT2. Extra power loss associated with spurious turn-on could harm the device in either case. The reliability of the converter would be less, there could be large associated electro-magnetic noise.

5.3 *Design of Pulse Transformer for SiC Mosfets*

It is clear from Fig. 6 that despite having large value of self-inductance in each winding along with excellent coupling coefficient (see Table 3), both PT1 and PT2 were found not to be suitable for driving SiC Mosfets in parallel even for single-switch low-noise resonant converter. Due to small gate threshold voltage, at turn off, oscillations in gate voltage caused by parasitic inductance (l_{lk} of PT plus the stray inductance of GDC) while discharging the device capacitances C_{gs} (gate to source) and C_{gd} (gate to drain) can take a SiC Mosfet into the active region, resulting in spurious turn-on. When PT1 or PT2 was used, in either case during turn-off, there was spurious turn-on of Q1 and large ringing was noticed in both the gate voltages, and also in voltage and current of Q1. It appears to be complex to design a PT-based GDC to feed the desired narrow band asymmetrical gate voltage accurately and robustly to turn-on and turn-off multiple SiC Mosfets in an isolated manner. The PT needs to be close to an ideal one where l_{lk} plays critical role at turn of devices for suppressing any noise at the respective gate. The layout of the GDC also plays important role, its stray inductance should be small. The design of a PT should have large value of L_s with negligible l_{lk} in each winding.

5.4 Reducing Leakage Inductance of a Pulse Transformer

It was practically analyzed that to ensure current sharing among parallel SiC Mosfets, the PT should have large value of self-inductance L_s in each winding along with excellent value of *k*. And for handling gate voltage robustly during transient conditions, the value of l_{lk} should be negligible, it depends on winding layout, core material etc. [20], [21]. The value of l_{lk} depends on the leakage flux available in the core window. Understanding the factors that influence the value of l_{lk} is important. Its value between any two windings can be determined by using the expression:

$$l_{\mathrm{lk}} = \frac{\mu_0 N^2 l_{\mathrm{mt}}(\sum h + \sum w)}{3b_w}\frac{1}{m^2} \quad (13)$$

N is the number of turns of the winding, l_{mt} is the mean length per turn, *m* is the level of interleaving, $\sum h$ is the sum of the heights of all windings, $\sum w$ is the sum of the widths of the spacing gaps between winding layers, b_w is the bobbin winding breath. For a 1:1:1 ratio transformer, the number of turns *N* in each winding is,

$$N = \frac{V.\mu s}{BA_{\mathrm{c}}} \quad (14)$$

Considering the value of $k \approx 1$, the self-inductance of each winding, like l_{lk}, also varies with N^2, like,

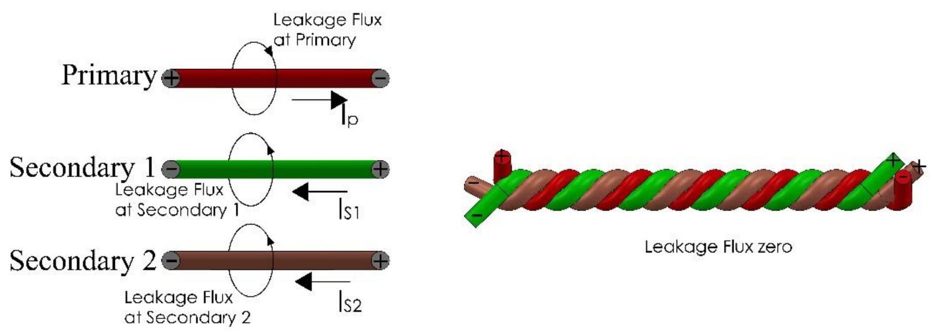
$$L_{\mathrm{p}} \approx L_{\mathrm{s1}} \approx L_{\mathrm{s2}} = N^2 A_{\mathrm{L}} \quad (15)$$

A_L (nH/turn) is the inductance factor of the chosen core.

5.5 Configuring a 3-Winding PT for SiC Mosfets

Though l_{lk} is significantly reduced by reducing the leakage flux through interleaving, large value of *m* increases the complexity of windings and increases the values of $\sum w$, $\sum h$ and l_{mt}, it gets more complicated for a 3-winding PT. In this research the objective is to design a simple, compact, and low-cost PT-based-GDC that can effectively drive two parallel SiC Mosfets Q2 and Q3 (Fig. 5) through introduction of requisite voltage isolation for proper use of the respective Kelvin source terminals. It does not need large isolation voltage V_{iso} among windings. If the magnetizing current of PT is neglected i.e., when self-inductance L_p (15) of primary winding is large, then the condition $I_{p1} = I_{s1} + I_{s2}$ is true. In the proposed PT, instead of interleaving (Fig. 7a), three minimally insulated or single-enameled conductors consisting of one primary and two secondary windings are bunched and twisted to make like a 3-conductor litz-wire (Fig. 7b). The summation of current in three-conductor litz-wire bunch would always be zero; it ideally does not create any flux around. When such conductor bunch is wound on the core like a single winding then the value of leakage flux of any wingding is inherently cancelled out; the value of l_{lk} of each winding would ideally be negligible.

The choice of core also plays a vital role for design of a PT for SiC Mosfets. For accurate control of asymmetrical voltage, the values of L_p, L_{s1} and L_{s2} and k should be large. On the other hand, to reduce the value of l_{lk}, the value of N should be small (13). Increase in core area A_c and/or the choice of low-loss core material having high value of saturation flux density and relative permeability would help reduce the value of N. To increase the value of k the core should have large A_L (nH/turn) where un-gapped core with large value of relative permeability is preferred. Though, nanocrystalline cores would be ideal [30], but due to the poor availability of miniature size nanocrystalline cores, toroidal shaped ferrites with large value of effective permeability are used here.



a) b)

Fig. 7: a) Each of three separate windings wire would have leakage flux around, the value of l_{lk} would be definite, and, b) 3-conductor litz-wire like single winding would have ideally zero leakage flux, hence minimum leakage inductance, any conductor could be used as primary or any secondary.

a) b)

Fig. 8: a) PT3: Conductors of three windings are wound one after the other (see Fig. 7a), and, c) The proposed PT4: 3-conductor litz-wire wound as a single winding (see Fig. 7b).

For comparative study, two PTs were designed and manually wound using a coated toroidal core (T1807, material grade: CF197) with core area A_c of 22.2 mm^2 and A_L value of 4500 nH/turn. The newly constructed PTs are shown in Fig. 8. Various parameters of each PT are listed in Table 4. It is clear that compared to PT1-PT3, the value of l_{lk} is minimum in the proposed PT4. The value of l_{lk} in PT3 is comparable with PT1 and PT2 (Table 3). The parametric values of PT4 are excellent with virtually having no deviation in winding parameters; primary and secondary windings could interchangeably be used.

Table 5: Parameters of PT with different winding layout

	PT3	PT4 (proposed)
V.µs rating	100	100
Turns ratio	16:16:16	16:16:16
Winding layout (dia. of wire of each winding: 0.3mm)	Wound like a transformer with no insulation layer placed in between [21]	Conductors of 3 windings were bunched like a litz wire, then wound like a one winding
V_{iso}, kV	>0.3	>0.3
L_p, L_{s1}, L_{s2}, mH	1.07, 1.067, 1.067	1.15, 1.15, 1.15
l_{pl}, l_{s1}, l_{s2}, µH	0.32, 0.32, 0.34	0.17, 0.17, 0.17
Capacitance, pF	≈30	≈30

5.6 *Experimental Results*

After analyzing the results of using PT1 and PT2 (Fig. 6), it was presumed that with similar or worse values of l_{lk} the performance of the converter using PT3 (see Table 4) would not be any better. Therefore, requisite experimentation was carried out using the proposed PT4. The experimental set up of single-switch resonant power converter is shown in Fig. 9. The major parameters of the power converter are listed in Table 5. Originally, the design and layout of the converter PCB could accommodate PT1 and PT2. Therefore, as shown in Fig. 10, due to different geometrical shape and winding termination, PT4 was kept hanging. The extra inductance value caused by overhang wires from each winding of PT4 were included in l_{lk} of Table 4.

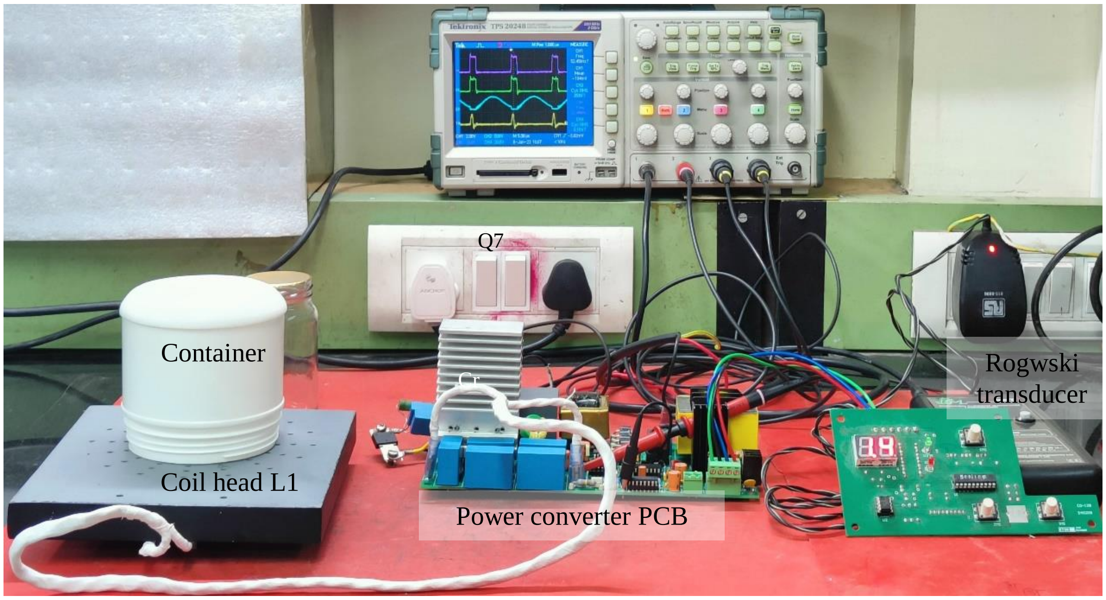


Fig. 9: Complete experimental set up.

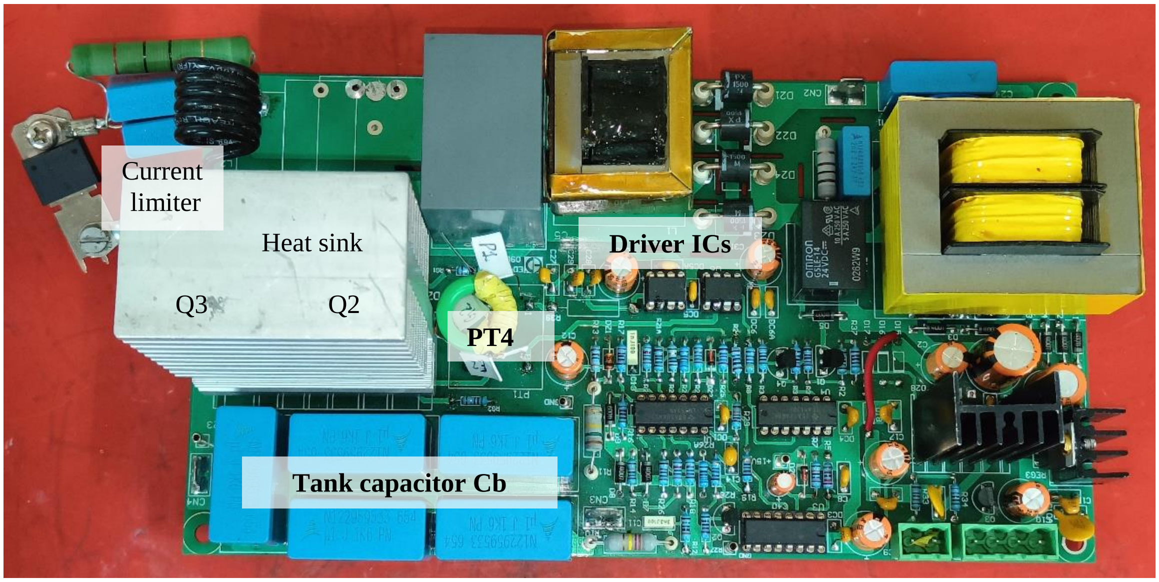
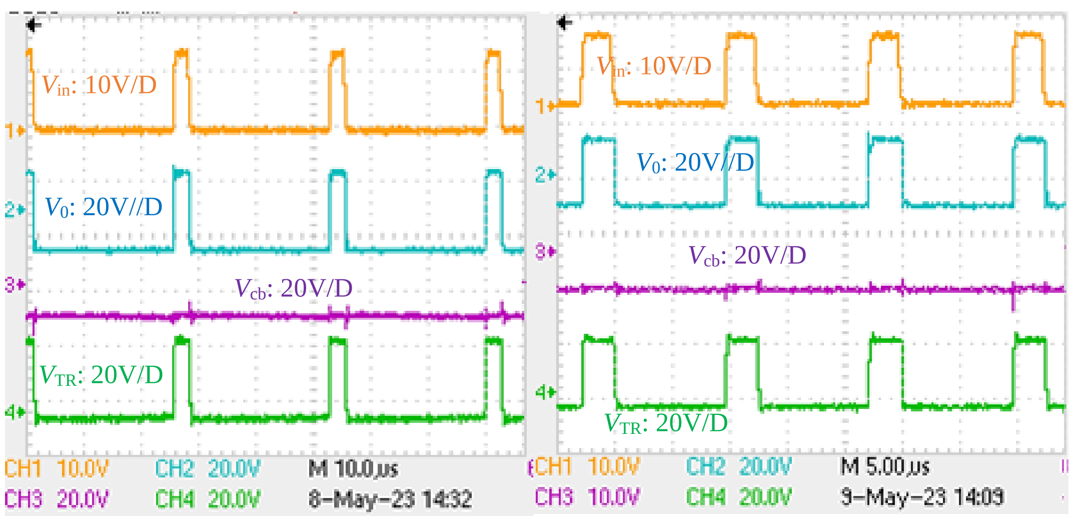


Fig. 10: Control, gate drive and power circuit in one printed circuit board.

Fig. 11 shows two sets of waveforms of various signals (as detailed in Table 2) of the primary side of PT4 based GDC (Fig. 5) at two extreme ends of operating frequency range of the converter. Each signal closely matched with the calculated results listed in Table 2.

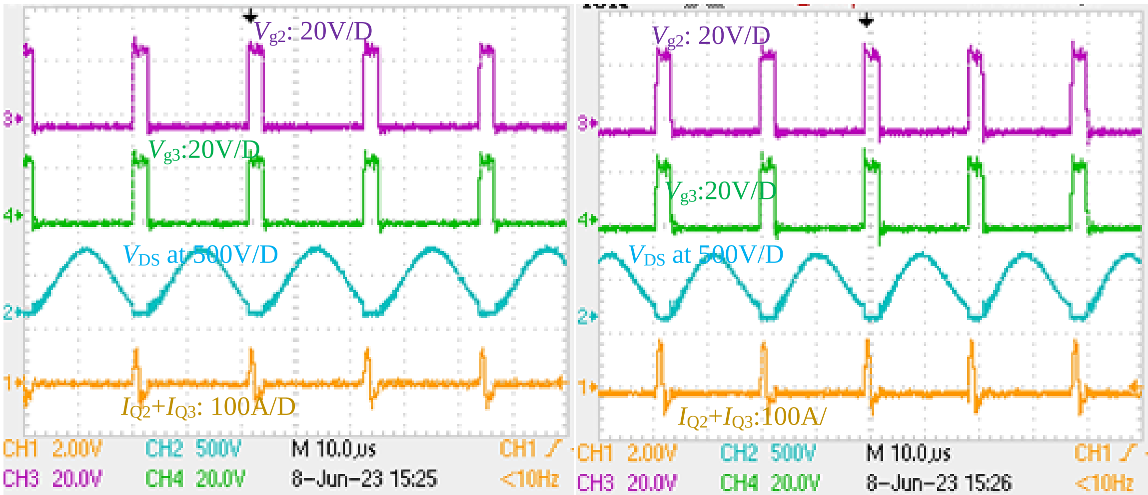
The mechanical system of automated capless induction sealing system is extremely complex and elaborate. Therefore, the PT-based power converter was validated in traditional cap sealing applications.



a) b)

Fig. 11: Primary side waveforms of the proposed PT4 for an input pulse having duty cycle of, a) 11% at 37 kHz, and, b) 24.3% at 81 kHz.

Fig. 12a shows a set of waveforms while performing traditional induction cap sealing using 55 mm diameter foil. The corresponding sealed container is shown in Fig. 13a. Fig. 12b shows waveforms while sealing using 95 mm foil. The corresponding sealed container is shown in Fig. 13b. It is clear from the waveforms of Fig. 12, belonging to two applications, that a PT wound in a single layer using 3-conductor litz-wire type bunching could virtually eliminate the ringing of gate voltage of Q2 and Q3 to avoid their spurious turn on. The results would further be improved when the stray inductances, particularly of Q3 (Fig. 10), are reduced through improved PCB layout.



a) b)

Fig. 12: Waveforms of two-SiC-Mosfet based power converter for induction sealing using the proposed PT4 when the coil was loaded, a) for sealing 55 mm foil, and, b) for sealing 95 mm dia. foil.

a) b)

Fig. 13: Sealed containers, a) foil diameter: 55 mm, and b) foil diameter: 95 mm.

The air circulation inside the enclosed converter was ensured by a 3-inch fan. For thermal load testing, a metal pan filled with water was considered as load. The set load (equivalent to worst case sealing load) was emulated by adjusting the distance between the coil and the pan. The ON-OFF duty cycle (5.0 sec ON, 0.5 sec OFF) was 91%. After two-hour thermal load cycling, the steady-state temperature recorded in heat sink was 60 ^{0}C. For IGBT based system (Section 4.2), though the heat was 33% larger, the steady state temperature was high at 80 ^{0}C. The ambient temperature was 35 ^{0}C.

6. Kindly attach drawings, reports, papers, charts or other materials that may aid in your description.

Following documents are attached in this submission:

1. Fig.1: Sealed containers using induction heating principle.
2. Fig. 2: Schematic diagram of a single switch induction heating controller
3. Fig. 3: Two sets of waveforms of charging the tank circuit in IGBT based single-switch controller

4. Fig. 4: Waveforms of IGBT based power controller while sealing in two different applications
5. Fig. 5: Diagram of a PT based GDC for driving two SiC Mosfets in parallel.
6. Fig. 6: Even when the coil was not loaded, large ringing in gate voltages during turn-off effected spurious turn-on of SiC Mosfets while using, a) PT1, and, b) PT2.
7. Fig. 7: Winding pattern in a pulse-transformer, a) Conductor of any winding would have leakage flux around, and, b) 3-conductor litz-wire placed like a single winding would have ideally zero leakage flux, hence minimum leakage inductance.
8. Fig. 8a: PT3: Conductors of three windings are wound one after the other; Fig. 8b: The proposed PT4: 3-conductor litz-wire wound as a single winding.
9. Fig. 9: Complete experimental set up.
10. Fig. 10: Control, gate drive and power circuit in one printed circuit board.
11. Fig. 11: Primary side waveforms of the proposed PT4 for an input pulse having duty cycle of, Fig. 11a) 11% at 37 kHz, and, Fig. 11b) 24.3% at 81 kHz.
12. Fig. 12: Waveforms of two SiC Mosfets based power converter for induction sealing using the proposed PT4 when the coil was loaded, a) for sealing 55mm foil, and, b) for sealing 95 mm dia. foil.
13. Fig. 13: Sealed containers, a) foil diameter: 55mm, and b) foil diameter: 95 mm.
14. Two test reports of the equipment with the proposed coil for 55 mm and 95 mm diameter foil.

7. What are the aspects of your disclosure that you want to claim/monopolize?
Proposed Claims: This invention addresses following features:

1. This invention proposes to use a novel three-winding pulse transformer to be an integral part of a gate drive circuit capable of driving two SiC Mosfets in parallel in an isolated manner for a single-switch induction heating power controller not only for traditional cap sealing, but also for capless sealing applications
2. Due to their low switching and conduction power losses and superior thermal behavior SiC Mosfets are preferred as a switch so that the power controller could be used almost like a continuous duty converter, with very small OFF time
3. To make the gate drive circuit compact, pulse transformer was used for both galvanic isolation as well as for driving both the SiC Mosfets that need accurate asymmetrical gate voltage for turn-on and turn-off
4. To make the gate driving compact, pulse-transformer based gate drive circuit does not need any separate power supply (uni-polar or bi-polar) for GDC
5. For feeding the asymmetrical gate voltage accurately and robustly, the proposed pulse transformer has been designed so that each winding to possess large value of self-inductance as well as excellent coupling coefficient
6. To avoid any spurious turn-on of sensitive SiC Mosfets caused by oscillations or ringing in gate voltage, the novel winding construction of the proposed transformer possesses negligible value of leakage inductance in each winding
7. In the novel pulse-transformer design, the leakage inductance in each winding is drastically reduced by converting three conductors of three windings into a single litz-wire like conductor by bunching and twisting the conductors of each winding.
8. In the novel pulse transformer, the litz-wire like three-conductor bunch is wound on the core like a single winding as wound for an inductor that not only produces minimum leakage inductance in all the three windings, their value would be same, thereby, any wire could be used either for primary or any secondary.

9. The isolation voltage of the proposed winding configuration is sufficient to avail the feature of Kelvin source terminals to have noise free gate driving of SiC Mosfets operating in parallel, the novel pulse transformer based gate drive has been completely validated for single switch induction cap sealer.

8. Have you conducted novelty/inventiveness search for your invention? If yes, what are the databases /references used by you? What are the search results?

We believe in creating products for the global market. We are a global player in induction cap sealing business and we have taken part regularly at several international events such as Interpack Dusseldorf, Germany. Four of our models have won The National Awards for Excellence in Packaging from Indian Institute of Packaging. Patents were granted to two of our innovations on induction cap sealing and another was for induction heating. We are fully aware of product profile of all competitors globally, plus, we are aware of the world market. We have dedicated Research & Development wing to innovate and enrich our product profile in cap sealing. It is recognized by DSIR, Govt. of India. One of our products on Induction Cap Sealing won the prestigious The National Technology Awards 2023 (MSME category) from Science and Technology Ministry. Moreover, we have done extensive search on Google Patents, articles available on IEEE, Elsevier, Google, ResearchGate, Semantic Scholar, etc. Our Technical Director Mr. Arun Kumar Paul is a Senior Member of IEEE and he attends IEEE and other international conferences regularly.

9. Do you feel that a person of "average" skill (not-extraordinary skill) in your area of technology would have arrived at your invention with existing knowledge in public domain? If no, what could be the reasons for the same?

Not likely. This invention needs deep knowledge in multi-disciplinary fields such as:

1. Electro-magnetic field theory to quantify the power transfer by induction effect
2. High-frequency power electronics controller
3. Static and dynamic characteristics of SiC Mosfets, etc.
4. The gate drive requirements and impact of turn-off transients of SiC Mosfets
5. Impact of transformer-based isolated gate drive circuit on the gate characteristics of SiC devices.

10. Kindly provide broad workable ranges for all the parameters involved in your invention.

The proposed isolated GDC could be used for several other applications such as,

1. In all applications where the duty cycle is moderate
2. Could comfortably be used for Si IGBT or Mosfet for wide range of duty cycle
3. Ideally suited to provide requisite isolation for effective use of the Kelvin source terminals for parallel connected SiC Mosfets, in particular, and for Si switching devices in general.

11. References

[1] A. K. Paul, "Zero ventilated induction sealing device with improved spatial distribution of optimized power loss", Indian Patent 415961, 2022. (the product received The National Technology Award 2023).

[2] A. K. Paul and S. Chinoy, "Induction sealing head and a coil assembly thereof for energy efficient sealing of containers" Indian Patent 425208, 2023.

[3] K. J. Herzog "Multiple head induction sealer apparatus and method", US Patent, 2001.

[4] A. K. Paul and S. Chinoy, "Air cooled induction heater for efficient sealing of containers using wide range foils," *IEEE Trans. Ind. Appln.*, vol. 52 (2), pp. 3398-3407, Jul./Aug. 2016.

[5] A. K. Paul, “Zero-ventilated self-cooled induction heating device: Topology and component engineering,” *J Power Electron. Devices and Components*, Open Access, vol. 3, pp. 1-10, 100013, 2022.
[6] H. W. E. Koertzen, et al, "A comparative study of single switch induction heating converters using novel component effectivity concepts," *Conf. Record IEEE PESC '92*, vol.1, pp. 298-305, 1992, IEEE.
[7] X. Li, et al, "Understanding switching losses in SiC MOSFET: Toward lossless switching," *Conf. Proc. IEEE WiPDA*, Blacksburg, VA, USA, 2015, pp. 257-262.
[8] X. She, et al, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193-8205, Oct. 2017.
[9] A. Anthon, et al, "Switching investigations on a SiC MOSFET in a TO-247 package," *Conf. Proc. IECON 2014*, Dallas, TX, USA, 2014, pp. 1854-1860.
[10] K. H. Cha, C. T. Ju and R. Y. Kim, “Analysis and evaluation of WBG power device in high frequency induction heating application”, *Energies*, 13(20), p.5351, MDPI, 2020.
[11] J. Rice and J. Mookken, "SiC MOSFET gate drive design considerations," 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), Chicago, IL, USA, 2015, pp. 24-27.
[12] G. Yu, et al, "A transformer isolated driving method for SiC MOSFETs with a constant negative off voltage," *Conf. Proc. IEEE PEMC*, Gliwice, Poland, 2021, pp. 39-45.
[13] Q. Qian, J. Yu, J. Zhu, W. Sun and Y. Yi, "Isolated gate driver for SiC MOSFETs with constant negative off voltage," *Conf. Proc. 2017 IEEE APEC*, Tampa, FL, USA, 2017, pp. 1990-1993.
[14] J. Garcia, et al, "Self-powering high frequency modulated SiC power MOSFET isolated gate driver," *IEEE Trans. Ind. Applns*, vol. 55, no. 4, pp. 3967-3977, July-Aug. 2019.
[15] Y. Yang, Y. Wen and Y. Gao, "A novel active gate driver for improving switching performance of high-power SiC MOSFET modules," *IEEE Trans. Power Electron*., vol. 34, no. 8, pp. 7775-7787, Aug. 2019.
[16] A. P. Camacho, et al, "A novel active gate driver for improving SiC MOSFET switching trajectory," *IEEE Trans. Ind. Electron.*, 64 (11), pp. 9032-9042, Nov. 2017.
[17] B. Zhang, et al, "A magnetic coupling based gate driver for crosstalk suppression of SiC MOSFETs," *IEEE Trans. Ind. Electron*., 64(11), pp. 9052-9063, Nov. 2017.
[18] K. S. Muhammad and D. D. -C. Lu, "Magnetically isolated gate driver with leakage inductance immunity," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1567-1572, April 2014.
[19] V. Nguyen, et al, "Compact, isolated and simple to implement gate driver using high frequency transformer," *Conf. Rec. 26th IEEE APEC*, Fort Worth, TX, USA, 2011, pp. 1092-1098.
[20] P. Scoggins, “A guide to designing gate-drive transformers,” *Power Electronics*, 2007.
[21] Z. Ouyang, J. Zhang and W. G. Hurley, "Calculation of leakage inductance for high-frequency transformers," *IEEE Trans. Power Electron*., vol. 30, no. 10, pp. 5769-5775, Oct. 2015.

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14. Any additional notes or remarks.

The performance of the proposed GDC based power converter would further improved if following measures are taken:

1. By using SiC Mosfets with higher value of gate threshold voltage
2. By reducing the stray inductance of the GDC through improved PCB layout
3. By choosing superior core material with higher value of relative permeability, higher value of saturation flux density and much reduced value of core loss density. Such core would need lesser number of turn.